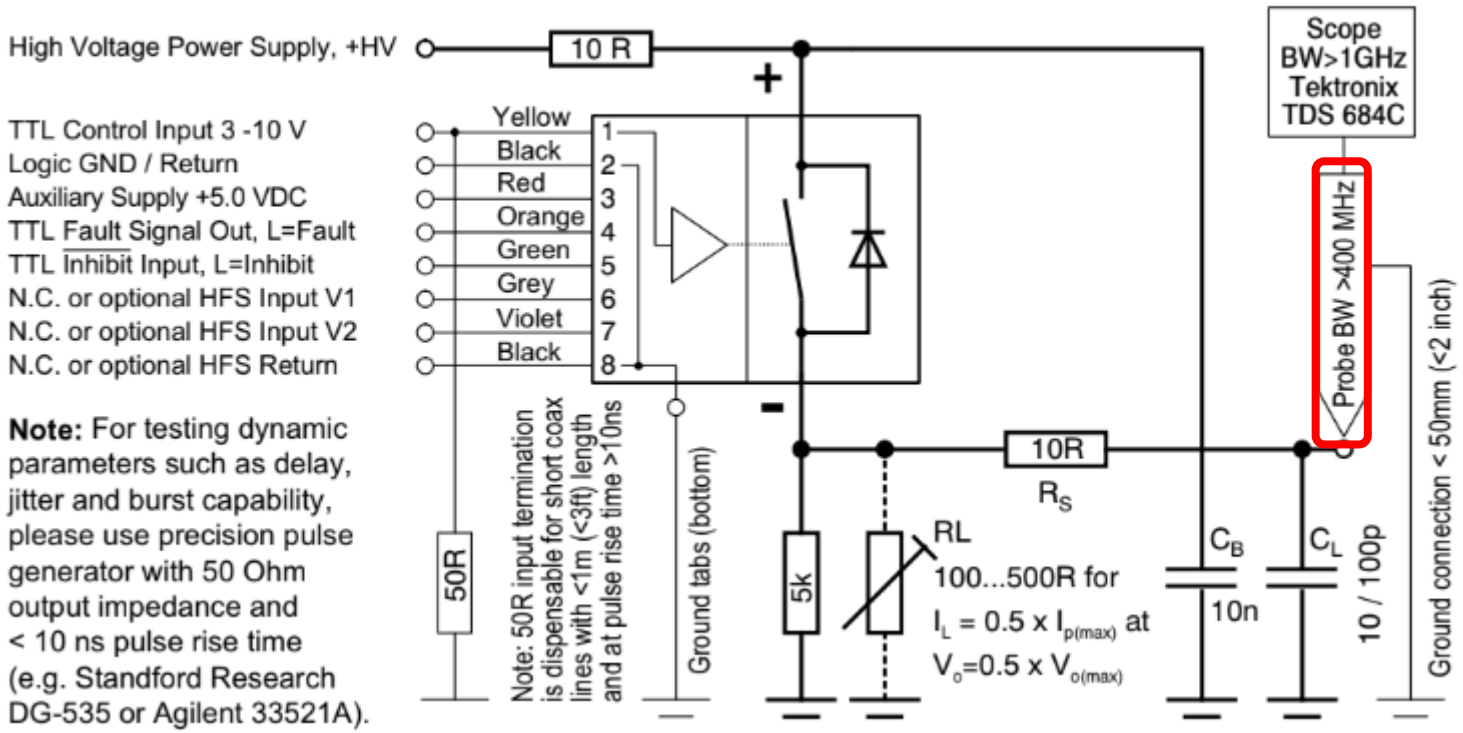
Trap

HV probe

박관형

HV switch

Test Circuit (High-Side Switch)



5 ns Rise Time • 3 MHz Rep Rate
6 MHz Burst • $t_{(on)}$ = 50 ns ... ∞

HV probe (6 kV)

Teledyne LeCroy HVP120

Price Break	Unit Price	Extended Price
1	407.00000	$407.00

Specifications

Electrical Characteristics

Bandwidth	400 MHz
Risetime (10% - 90%)	900 ps (typical)
Maximum Input Voltage*	
Measurement Category II	1000 Vrms
Measurement Category I	4000V Transient Overvoltage at 1000 Vrms 6000V Transient Overvoltage at 0 Vrms
Pollution Degree*	2
Input Capacitance	7.5 pF (typical)
Compensation Range	10 pF - 50 pF (typical)
Attenuation Ratio	100:1 ± 2%

Environmental

Temperature (Operating)	0°C to 50°C
Temperature (Non-Operating)	-40°C to 71°C
Humidity (Operating)	80% RH (Non-Condensing) up to 31°C, decreasing linearly to 40% RH at 50°C
Altitude (Operating)	up to 2,000 m
Altitude (Non-Operating)	up to 15,000 m

General Characteristics

Weight (probe)	67 g (0.15 lbs)
Cable Length	2 m (6.56 ft)
Probe Tip Diameter	5 mm (0.20 inches)

** As defined in IEC 61010-031*

HV probe (6 kV)

가격 (KRW)

수량	단가
1	₩1,486,933.6

ELECTRICAL CHARACTERISTICS

System attenuation: 1000:1
System input resistance: 50 MΩ
Input capacitance: < 6 pF
Compensation range: 10 pF to 50 pF
System BW (-3 dB): 400 MHz typical
Max. non-destructive input voltage: 6 kV
See voltage derating curve

HV probe (39 kV)

CT4028
39 kV High Voltage Probe

Features:

- Input voltage of 39 kV (DC+ACpk)
- 220 MHz bandwidth
- Voltage dividing of 1000:1
- Frequency compensation

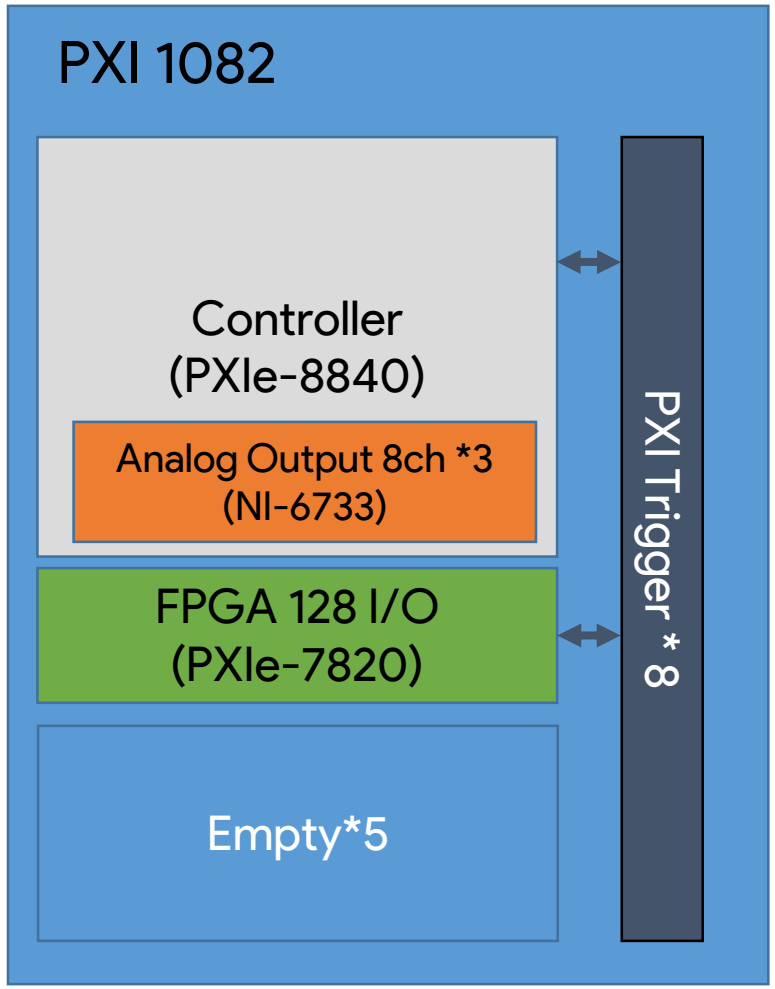
가격 (KRW)

수량	단가
1	₩980,100
25	견적

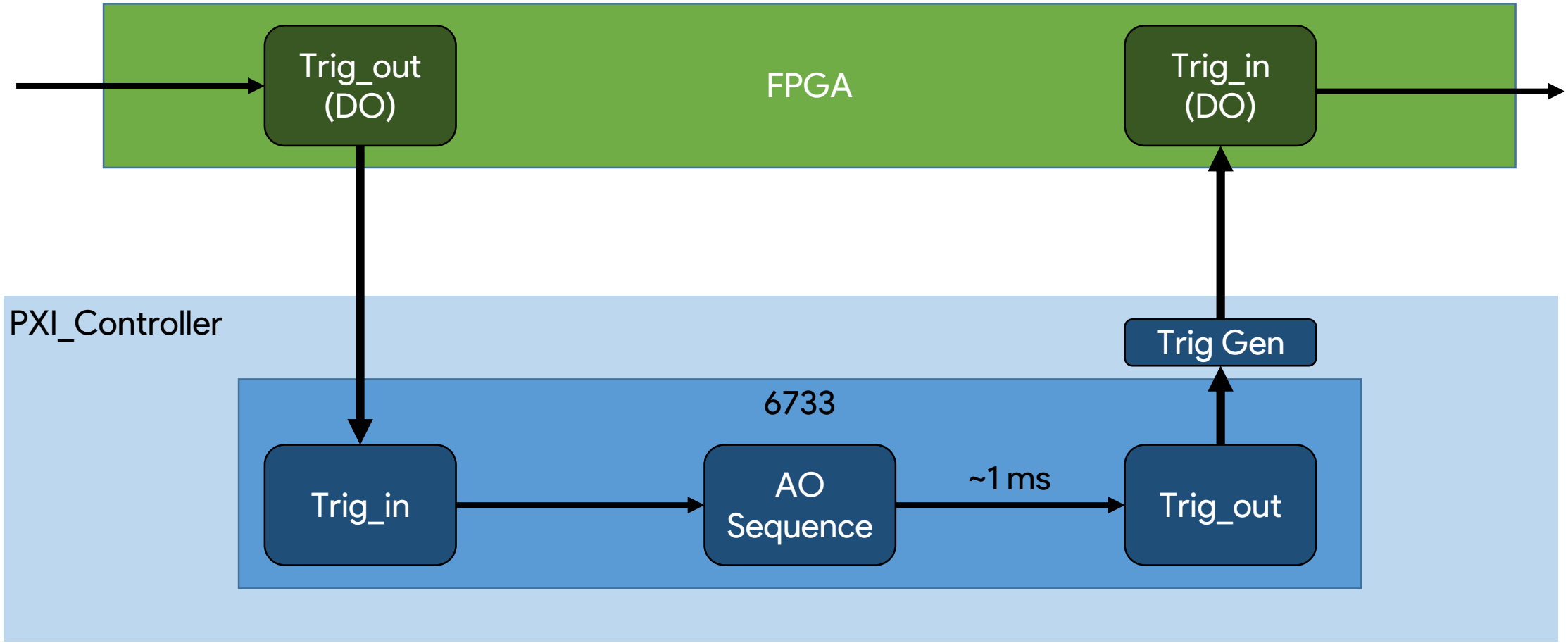
Specifications

Operating Parameters	
Maximum Input Voltage (CAT I)	39 kV (DC + ACpk) 27 kVrms AC
Maximum Loading	1000:1
Current	45 µA
Division Ratio	1000:1
Bandwidth	DC to 220 MHz
Compensation Range	10 pF to 35 pF
Temperature Coefficient	≤200 ppm/°C
Input Resistance	900 MΩ
Input Capacitance	2.0 pF
Rise Time	1.6 ns
Signal/Noise	> 60 dB @ 1 kHz > 50 dB @ 1 MHz
Accuracy	
DC Volts	≤3% (0 to 35 kV)
AC Volts	≤3% at 1 kHz

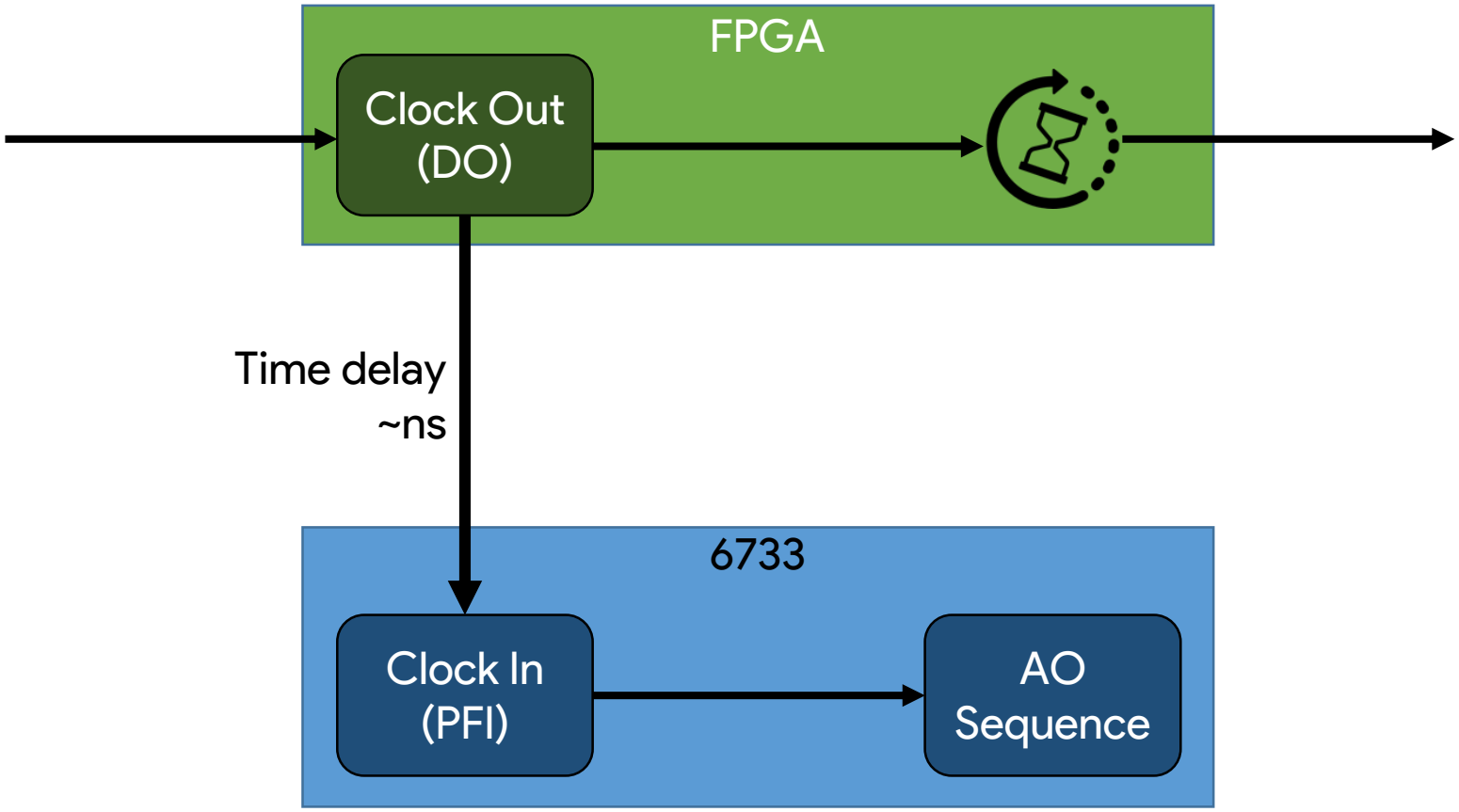
PXI


PXI 1082
Controller
(PXIe-8840)
Analog Output 8ch *3
(NI-6733)
FPGA 128 I/O
(PXIe-7820)
Empty*5
PXI Trigger * 8

FPGA – AO Timing



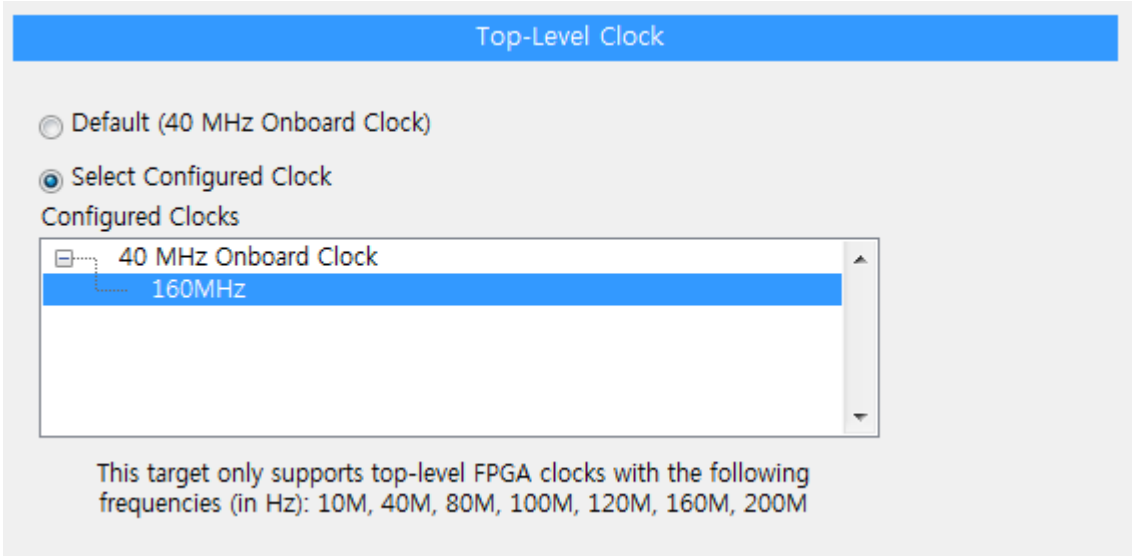
FPGA – AO Timing



Trap Sequence timing

Reconfigurable FPGA

FPGA type	Kintex-7 160T
Number of flip-flops	202,800
Number of LUTs	101,400
Embedded Block RAM	11,700 kbits
Number of DSP48 slices	600
Timebase	10, 40, 80, 100, 120, 160, or 200 MHz
Default timebase	40 MHz
Timebase reference source	PXI Express 100 MHz (PXIe_CLK100)
Timebase accuracy	±100 ppm, 250 ps peak-to-peak jitter
Data transfers	DMA, interrupts, programmed I/O
Minimum sampling period	5 ns



Joint experiment with Dirk

Dirk & KH

KH

Mon	Tue	Wen	Thu	Fri	Sat	Sun
27	28	29	30	31	1	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16